A 0.54 THz VCO in 40 nm bulk CMOS with 22 GHz tuning range

Wouter Steyaert and Patrick Reynaert
ESAT-MICAS, KU Leuven,
Kasteelpark Arenberg 10,
B-3001 Leuven, Belgium
Email: Patrick.Reynaert@esat.kuleuven.be

***Abstract*— This work presents a 540 GHz LC-VCO with buffer, implemented in a 40 nm bulk CMOS technology. The buffer is optimized for non-linear operation, to maximize the third harmonic generation at 540 GHz. The third harmonic is coupled to the load by a transformer. To accurately measure the output power, a WR-1.5 probe has been used. The output power is -31 dBm at 543 GHz, for 16.8 mW of DC power consumption. The output frequency can be tuned from 561.5 GHz to 539.6 GHz, resulting in a 21.9 GHz tuning range,the highest reported so far for CMOS THz oscillators. The 3-dB output bandwidth is 5.5 GHz.**

I. Introduction

With each new technology node, the f_{max} increases. This allowed the creation of many mm-wave circuits in CMOS. The upcoming interest in THz or sub-mm wave (300GHz to 3THz) applications, such as Tbps communication, imaging and sensing systems, requires circuits to operate above the f_{max} of current CMOS technologies. The f_{max} of a 45 nm bulk CMOS technology is approximately 310 GHz [1], making linear operation above this frequency impossible. However, it is still possible to generate signals above f_{max} by utilizing harmonics: the definition of f_{max} states that there is no power amplification above f_{max}, but this does not mean that there is not any power present at higher frequencies in the form of harmonics. By designing oscillators that utilize these harmonics, transmitters operating in the THz spectrum have been demonstrated [2] [3] [4] [5]. One of the major drawbacks of THz transmitters is the limited output power that is available at these high frequencies. To overcome this, the power of the harmonics can be boosted by different power combining techniques, such as linear superposition [6] or N-push oscillators [7].

Unfortunatley, this harmonic-oriented approach results in low power efficiency as the majority is "wasted" in the unwanted fundamental frequency. Additionally, there is also a limited tuning range in current THz oscillators. The design process is further complicated by the limited accuracy of simulation models in the THz region, as well as the increasingly dominant impact of a complicated network of parasitic components.

In this work a fully differential sub-mm wave VCO with large tuning range in a 40 nm bulk CMOS technology was fabricated and measured. The third harmonic, generated by the LC-tank and buffer, is coupled to the output by a transformer.

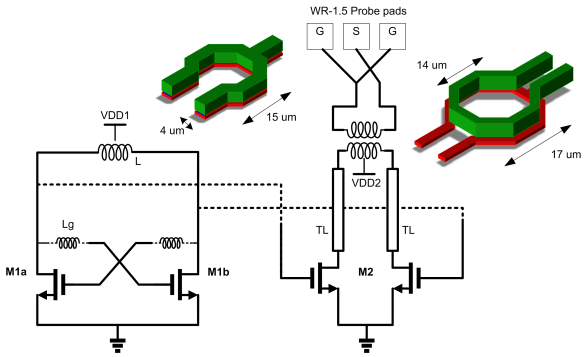


Fig. 1. Schematic of the VCO with WR-1.5 probe pads. The LC-tank consists of the inductor L and the parasitic capacitances

To get accurate measurements, a WR-1.5 probe and spectrum analyzer extender has been used.

II. Third harmonic generation and extraction from a LC VCO

The VCO consists of a resonating LC-tank, a cross-coupled transistor pair and a buffer to generate the third harmonic (Figure 1). In contrast to previous work [2]–[5], in this work the first stage is optimized for high power at the fundamental frequency f_{osc} = 180 GHz, whereas the second stage is optimized for high harmonic generation and transfer.

A. VCO core

As the f_{osc} is determined by the LC product of the tank, these values become very small for high oscillation frequencies. Therefore, the LC-tank of the VCO consists of a single-turn symmetrical inductor with center tap for the supply voltage. In many LC-VCO's, a varactor is placed between the drains of the cross-coupled transistors M1a and M1b for tuning the oscillation frequency by changing the total capacitance C in the LC-tank. The varactor has to be sufficiently large compared to the parasitic capacitances to effectively control the oscillation frequency. However, the values of the L and C should be small for a tank resonance at high frequencies. Also, the quality factor of varactors decreases with increasing frequency, which reduces the overall quality of the LC-tank. For these reasons, the tuning varactor was omitted from the LC-tank. The resulting C in the LC-tank is now the parasitic

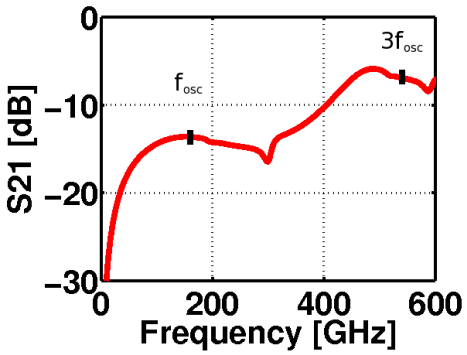


Fig. 2. Simulated S21 for the coupling structure to the probe pads

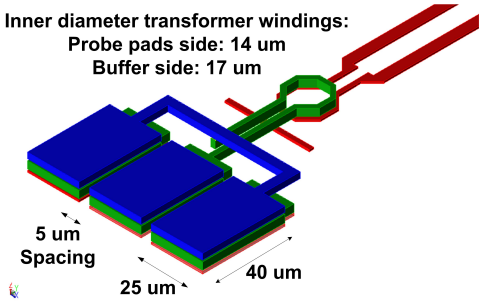


Fig. 3. Layout of the transmission lines, transformer and probe pads

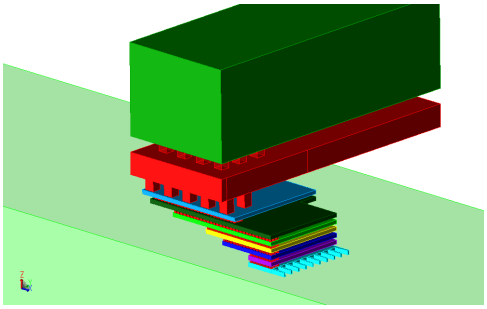


Fig. 4. Tapered via stack to minimize the C_d without introducing a large series resistance between the transistor drain and the inductor leads

capacitances of the buffer, cross-coupled pair, interconnect and the inductor itself. Tuning of the frequency is done by varying the supply voltage of the VCO core, VDD1, which changes the C_{gs} capacitance of the transistors. Besides capacitance for the tank, the cross-coupled pair provides a negative resistance to compensate the resistive losses in the inductor. As the generated negative resistance diminishes with increasing frequency, the size of the M1 transistors increases to adequately compensate the inductor losses. Unfortunately, larger transistors also increase parasitic capacitances, lowering the LC-tank's resonance frequency. By implementing series inductors in the cross-coupling connections, the performance of the M1 transistors is improved: this allows smaller transistor sizes for the same negative resistance at high frequencies, resulting in a smaller tank capacitance [8].

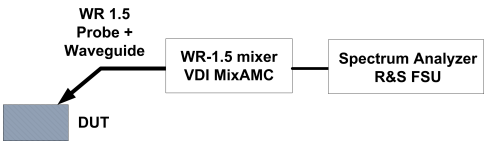
B. Buffer and transformer

Transistors M2 form the buffer that isolates the LC-tank from the load. The transistor size is kept small to reduce the capacitive loading of the LC-tank. To improve the generation of the third harmonic, a large voltage swing is applied at the gates of the buffer and the supply voltage of the buffer (VDD2) is chosen differently from the VCO core to improve non-linear operation. Simulations showed that a VDD2 of 650 mV resulted in the highest amount of power at the third harmonic.

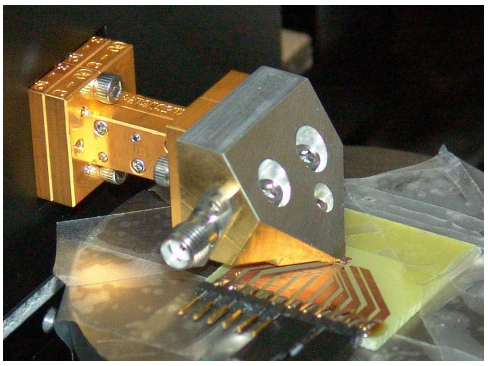
After generation, the third harmonic is coupled to the output using a transformer. The buffer transistors still have to operate at the fundamental frequency, as the third harmonic's power is related to the fundamental signal. The transformer thus has two purposes: (1) biasing and output matching of the buffer at the fundamental frequency on one side of the transformer, and (2) transferring the third harmonic to the probe pads on the other. To achieve this, the transformer was designed to have a good coupling of the third harmonic and is matched with the probe pads at 540 GHz. At the same time, the resulting transformer is conjugate matched with the output of the buffer at the f_{osc} of 180 GHz using high Z_0 (130 Ω) differential transmission lines. Simulations show that the whole coupling structure which starts at the drains of the M2 transistors favors the transfer of the third harmonic to the output over the fundamental frequency (Figure 2).

C. Implementation and design issues

Due to the small values of L and C, parasitic effects that are otherwise non-dominant can have a critical impact when designing sub-mm wave circuits. It is therefore important that the transistor models include this high-frequency behavior. While the f_{max} of a minimal 40 nm transistor is above 300 GHz, the practical limit on a transistor's speed will be lower due to the transistor size, layout and wiring. To maximize the f_{max} of M1 and M2, all transistors have double-contact gates to reduce the gate resistance R_g and narrow, 1 μm fingers. C_g and C_d of M1 form the majority of the capacitive part of the LC-tank. To reduce C_g, metals 3-6 were used in parallel for the cross-coupling connection of the M1 transistors, as lower metal layers would result in a larger C_{gb}. One important detail is the connection between the drain of the M1 transistors in the bottom metal layer and the leads of the inductor, in the top 2 metal layers. Using a small via stack straight to the top metals would keep C_d small, but would introduce a large series resistance. As this resistance would add to the resistive losses of the inductor, a larger negative resistance has to be generated to allow the oscillator to start up. A big via stack, on the other hand, would have a low series resistance but a large overlap of lower-layer metal and substrate, creating a large C_d and reduce the f_{osc} of the VCO. To tackle this dilemma, the via stack was given a tapered shape (Figure 4): narrower at the bottom, to minimize the metal-substrate capacitance, and getting wider to allow for more via's at higher metal layers, where the substrate coupling is less. Parasitic extraction and EM-simulations were done on interconnecting metals to model all layout-dependent parasitics as accurately as possible.



(a)



(b)

Fig. 5. Schematic overview of the measurement setup (a) and close-up of the WR-1.5 probe (b)

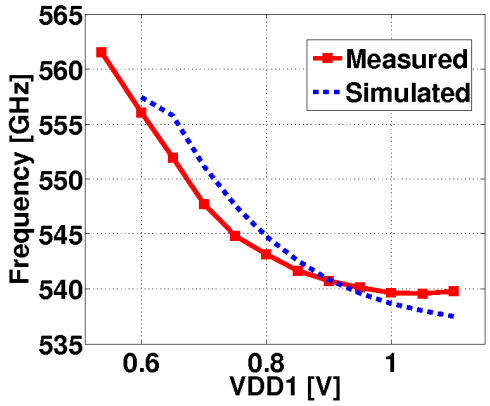
Lumped-component models of passive components become less accurate with increasing frequency. To accurately characterize these passives, a 2.5D EM-simulator (ADS Momentum) has been used to design the inductor, transformers, transmission lines and probe pads.

The single-turn inductor L (Figure 1) determines not only the inductance of the LC-tank, but also the resistive loss that the cross-coupled transistors have to compensate. By using the top two metal layers in parallel instead of only one metal layer, the series resistance of the inductor is reduced, as well as a small reduction in inductance. The inductor has an inner diameter of 15 μm and width of 4 μm, an inductance of 24.3 pH and a Q-factor of 22.9 at 180 GHz.

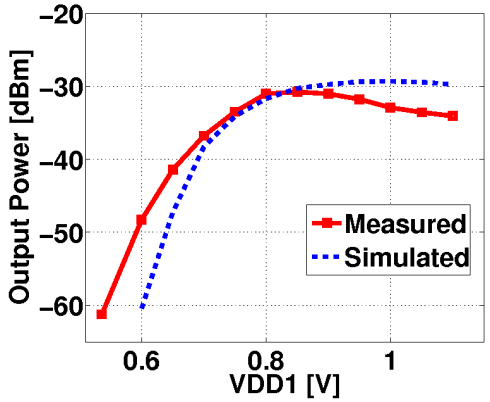
Figure 3 shows the layout of the probe pads connected to the output transformer and differential transmission lines. The transformer is implemented as two coupled single-turn inductors in the top two metal layers. The inductor on the buffer side includes a center tap for the biasing of the M2 transistors through the differential transmission lines. Each probe pad is 25 μm x 40 μm. While larger and longer probe pads make it easier for landing the probe tips, this will negatively impact the transfer of high-frequency signals as the probe pads form a parallel-plate capacitor with the substrate and also between the pads themselves.

III. Measurements

Measuring sub-mm wave signals is a challenging endeavor, as the high losses of the measurement equipment at these frequencies make it hard to detect the THz output signals. Other work at these frequencies uses a quasi-optic measurement approach: on-chip antennas radiate the signal into a Fourier-transform infrared spectroscopy (FTIR) system with sensitive, liquid nitrogen cooled bolometers to be able to detect the THz signals [2] [4] [5].



(a)



(b)

Fig. 6. Measured and simulated frequency tuning (a) and output power (b) for different supply voltages of the VCO core (VDD1). The buffer supply voltage (VDD2) is fixed at 650 mV

This work uses a high-frequency probe and mixer to accurately determine output frequency and power of the VCO. The measurement setup is shown in Figure 5. It consists of a WR-1.5 DMProbe attached to a VDI MixAMC with sub-harmonic mixer for the 500 GHz-750 GHz band. The output of the mixer is connected to a R&S FSU Spectrum Analyzer. The power measurements of the spectrum analyzer were validated with an Erickson PM4 power meter and a VDI AMC source module.

The results from measurements and simulation are shown in Figure 6. Measurements show good agreement with simulation results, indicating correct modeling of the passives and RF transistor's behavior at frequencies above f_{max}. When the supply voltage of the buffer, VDD2, is fixed at 650 mV, the VCO starts oscillating at 561.5 GHz for VDD1 = 540 mV. By changing the supply voltage of the VCO core, a 21.9 GHz tuning range is measured (539.6 GHz to 561.5 GHz). After de-embedding the losses of the probe and mixer, the peak output power is -31 dBm at 543 GHz, with a DC power consumption of 16.8 mW for a VDD1 of 800 mV. If the tuning range is limited to frequencies with an output power within 3 dB of the 31 dBm peak, the tuning range becomes 5.5 GHz, stretching from 539.6 GHz to 545.1 GHz. Due to the fully

TABLE I

COMPARISON WITH STATE-OF-THE-ART OSCILLATORS ABOVE 400 GHZ

Ref.	Harmonic	Frequency (GHz)	Tuning Range (GHz)	Output Power (dBm)	DC power (mW)	Measurement	Technology
This work	**3rd**	**543**	**21.9**	**-31**	**16.8**	**Probe**	**40 nm bulk CMOS**
[2]	2nd	410	2	-47	16.5	Antenna	45 nm bulk CMOS
[5]	4th	553	< 1	-36.6	64	Antenna	45 nm bulk CMOS
[3]	3rd	482	NA	-7.9	61	Probe	65 nm bulk CMOS
[9]	Fund.	573	< 1	-19.2	115	Probe	0.25 μm InP HBT

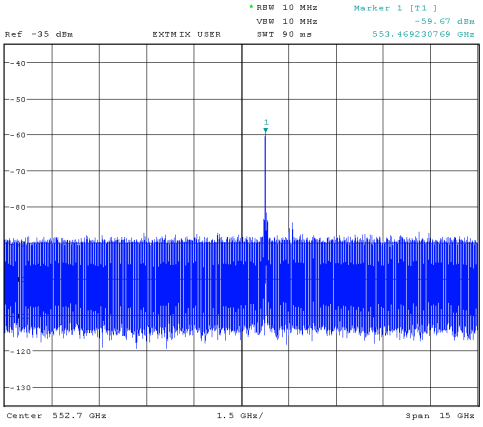


Fig. 7. Example of a measured output spectrum using a WR-1.5 probe, before de-embedding the loss of the probe, waveguide and external mixer

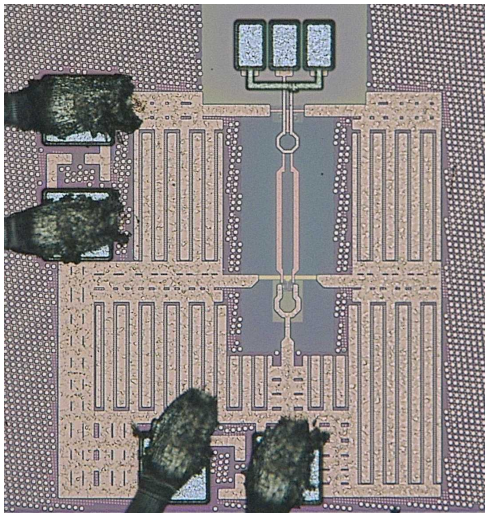


Fig. 8. Die photo of the VCO with WR-1.5 probe pads

differential approach, even harmonics are suppressed in favor of the uneven harmonics: the fourth harmonic at 730 GHz did not rise above the noise floor, meaning that it's output power is at least 30 dB lower than the third harmonic.

Table I compares the results with current state-of-the-art THz oscillators. To the authors knowledge, the total tuning range and 3-dB output bandwidth are the largest reported for CMOS oscillators above 400 GHz.

A die photograph is shown in Figure 8. The active area is 110 μm x 300μm, the total chip area including bond pads and decoupling is 350 μm x 430μm.

IV. CONCLUSION

This work presents a tunable oscillator at 543GHz, realized in 40 nm CMOS by generating and extracting the third harmonic of a LC-VCO using a buffer and transformer. Measurements showed a tuning range of 21.9 GHz, the widest range for CMOS oscillators above 400 GHz reported so far. The 3-dB output bandwidth is 5.5 GHz. WR-1.5 probes are used to accurately measure the peak output power, which is -31 dBm for a DC power consumption of 16.8 mW. The demonstrated VCO shows that THz oscillators above f_{max} with a wide tuning range are possible in bulk CMOS technologies.

REFERENCES

[1] W. Sansen, "Analog IC Design in Nanometer CMOS Technologies," in *VLSI Design, 2009 22nd International Conference on*, 2009, pp. 4–4.

[2] E. Seok, C. Cao, D. Shim, D. Arenas, D. Tanner, C.-M. Hung, and K. O, "A 410GHz CMOS Push-Push Oscillator with an On-Chip Patch Antenna," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, 2008, pp. 472–629.

[3] O. Momeni and E. Afshari, "High Power Terahertz and Millimeter-Wave Oscillator Design: A Systematic Approach," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 3, pp. 583–597, 2011.

[4] Q. Gu, Z. Xu, H.-Y. Jian, B. Pan, X. Xu, M.-C. Chang, W. Liu, and H. Fetterman, "CMOS THz Generator With Frequency Selective Negative Resistance Tank," *Terahertz Science and Technology, IEEE Transactions on*, vol. 2, no. 2, pp. 193–202, 2012.

[5] D. Shim, D. Koukis, D. Arenas, D. Tanner, and K. Kenneth, "553-GHz signal generation in CMOS using a quadruple-push oscillator," in *VLSI Circuits (VLSIC), 2011 Symposium on*, 2011, pp. 154–155.

[6] D. Huang, T. LaRocca, L. Samoska, A. Fung, and M.-C. Chang, "324GHz CMOS Frequency Generator Using Linear Superposition Technique," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, 2008, pp. 476–629.

[7] S.-C. Yen and T.-H. Chu, "An Nth-harmonic oscillator using an N-push coupled oscillator array with voltage-clamping circuits," in *Microwave Symposium Digest, 2003 IEEE MTT-S International*, vol. 3, 2003, pp. 2169–2172 vol.3.

[8] W. Volkaerts, M. Steyaert, and P. Reynaert, "118GHz fundamental VCO with 7.8% tuning range in 65nm CMOS," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2011 IEEE*, 2011, pp. 1–4.

[9] M. Seo, M. Urteaga, J. Hacker, A. Young, Z. Griffith, V. Jain, R. Pierson, P. Rowell, A. Skalare, A. Peralta, R. Lin, D. Pukala, and M. Rodwell, "InP HBT IC Technology for Terahertz Frequencies: Fundamental Oscillators Up to 0.57 THz," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 10, pp. 2203–2214, 2011.